GLOBALLY CLOCKED INTERFACES HAVING REDUCED DATA PATH LENGTH

Abstract

A interface, which connects memory and an integrated circuit, having a write path and read path that allow synchronous data propagation is provided. Further, a method for synchronizing data propagation through a read path and a write path of an interface is provided. The interface uses clock signals and paths based on a clock signal to synchronize the flow of data through various paths within the interface.

19443_2